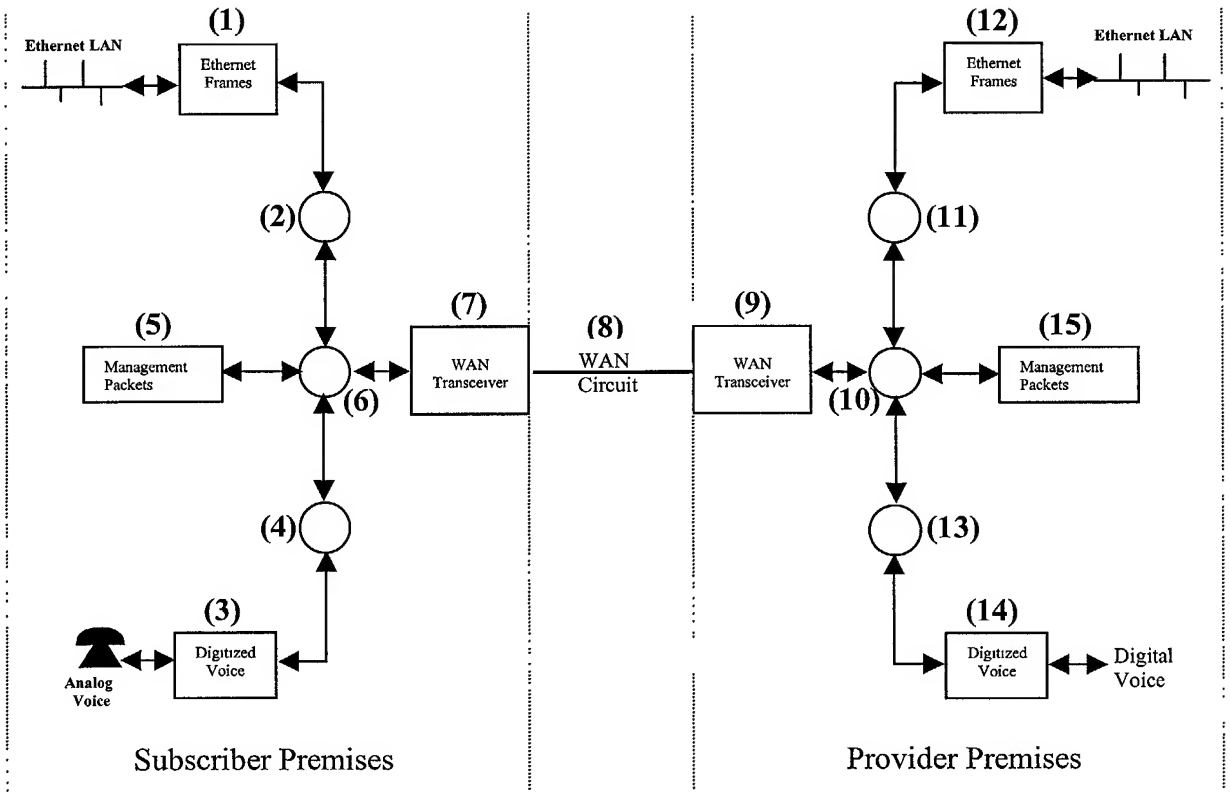
20220° 9h24h50OF

Figure 1. Data Flow Through the System



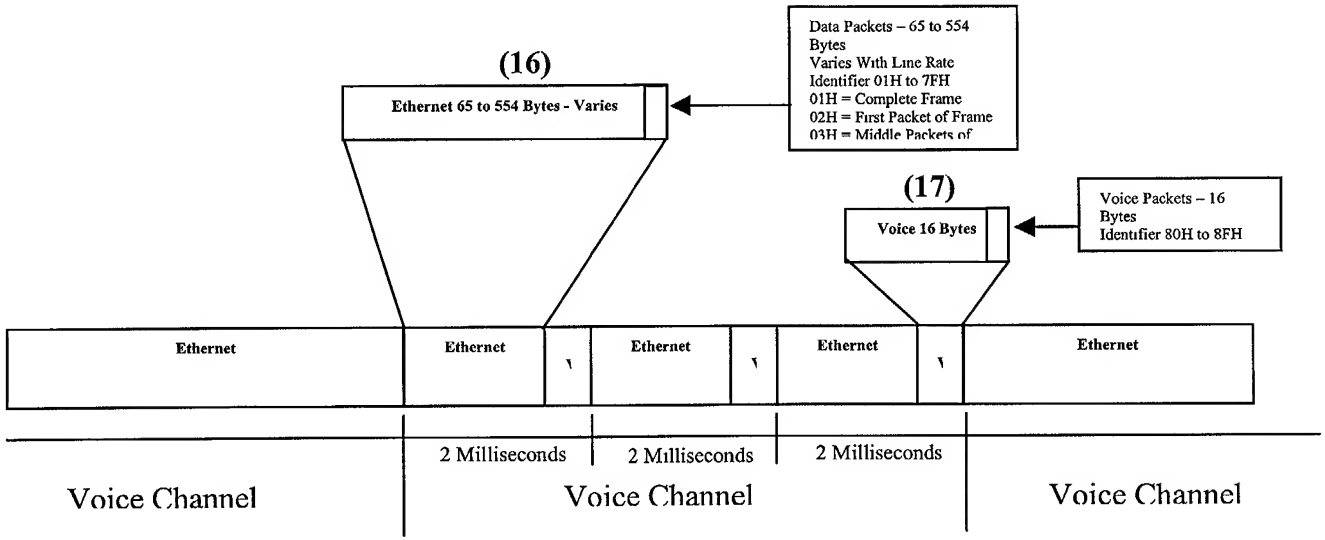


Figure 2. Packet Structure on the WAN Circuit

20020"9h2h500T

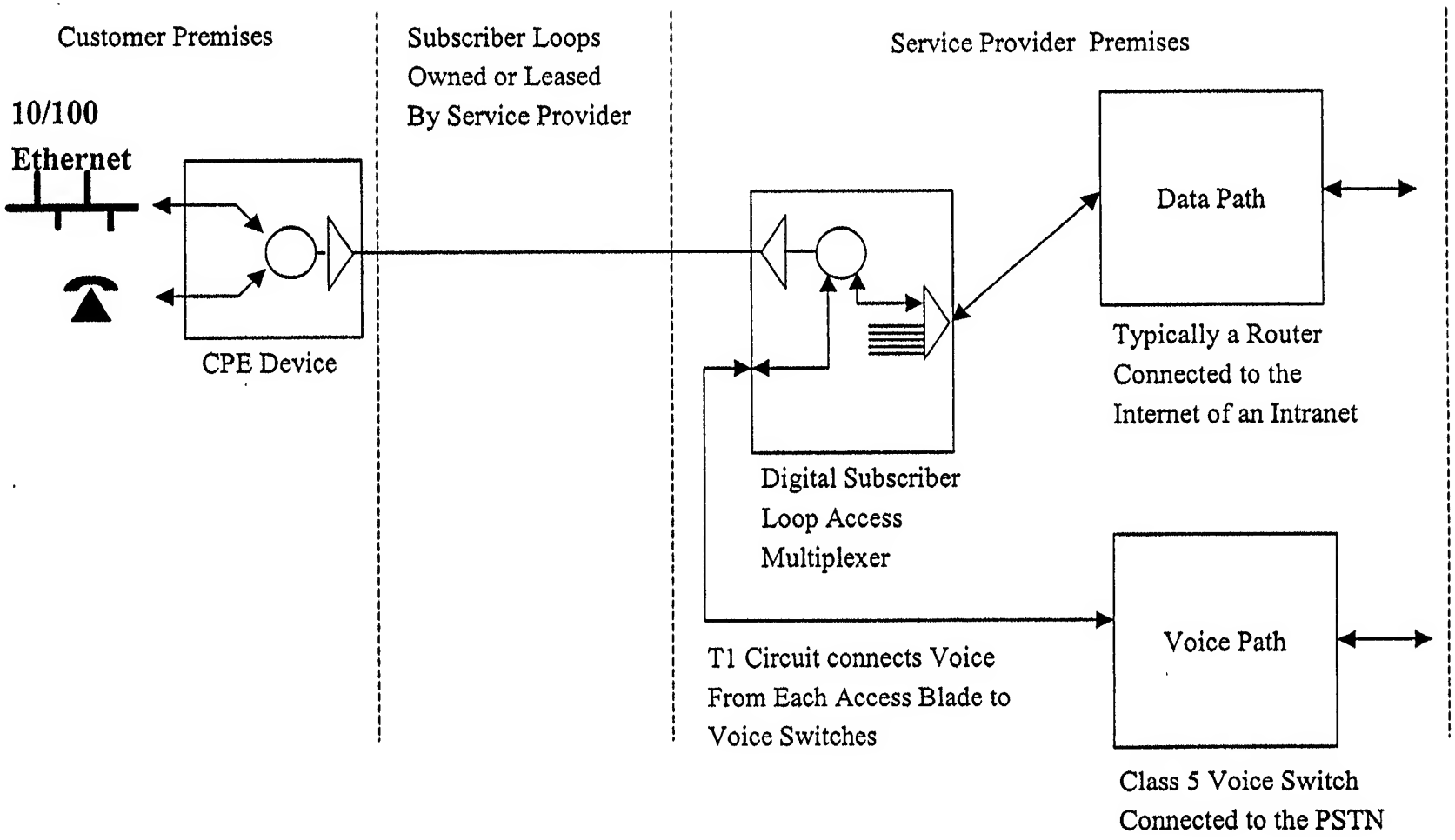


Figure 3

20E2F0" 9h2hS00T

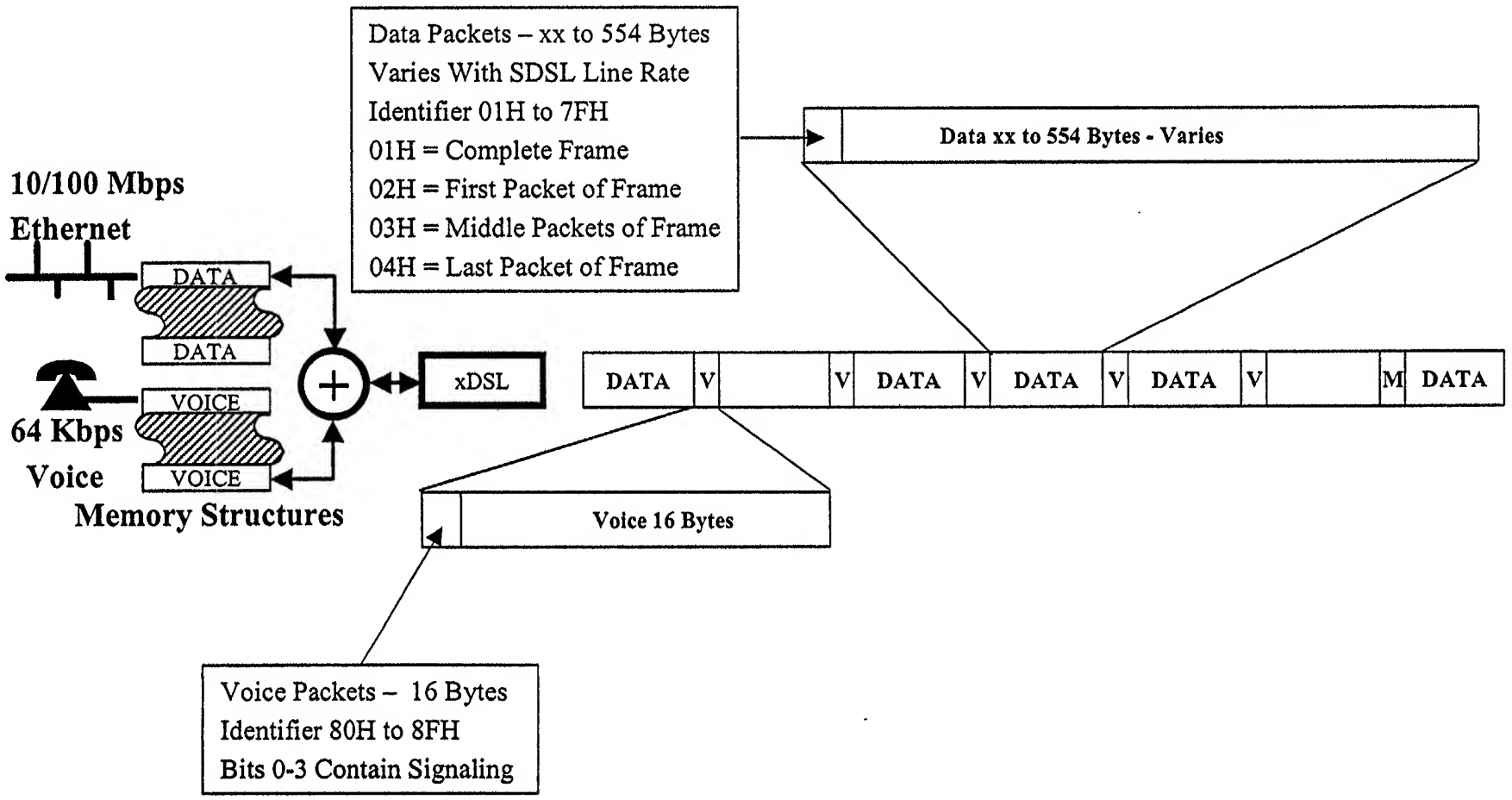


Figure 4

20220 9h2hS00F

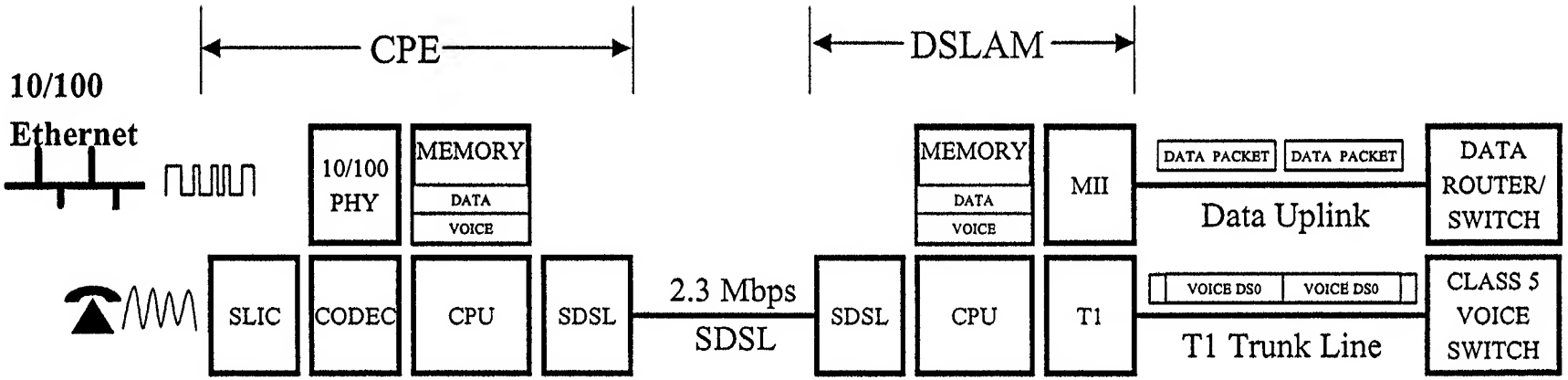


Figure 5

20020703 9h24m50f

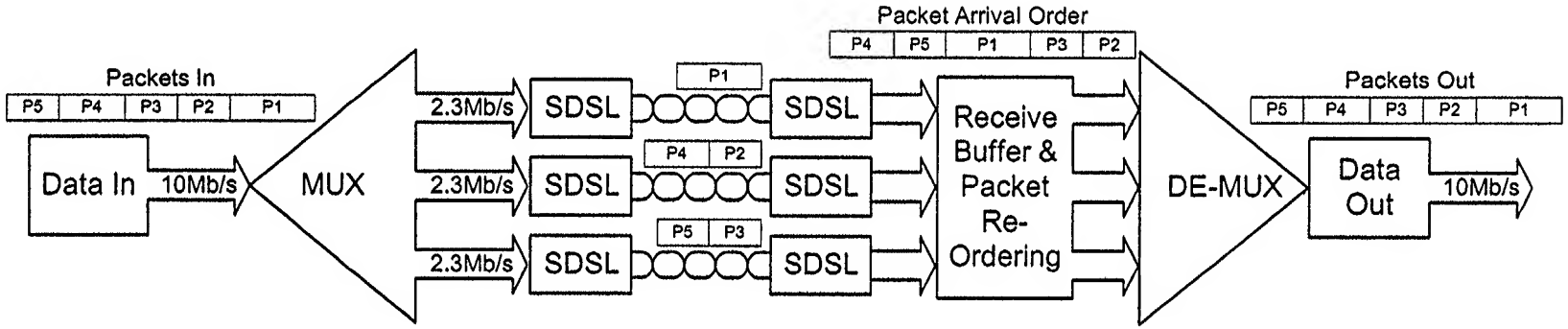
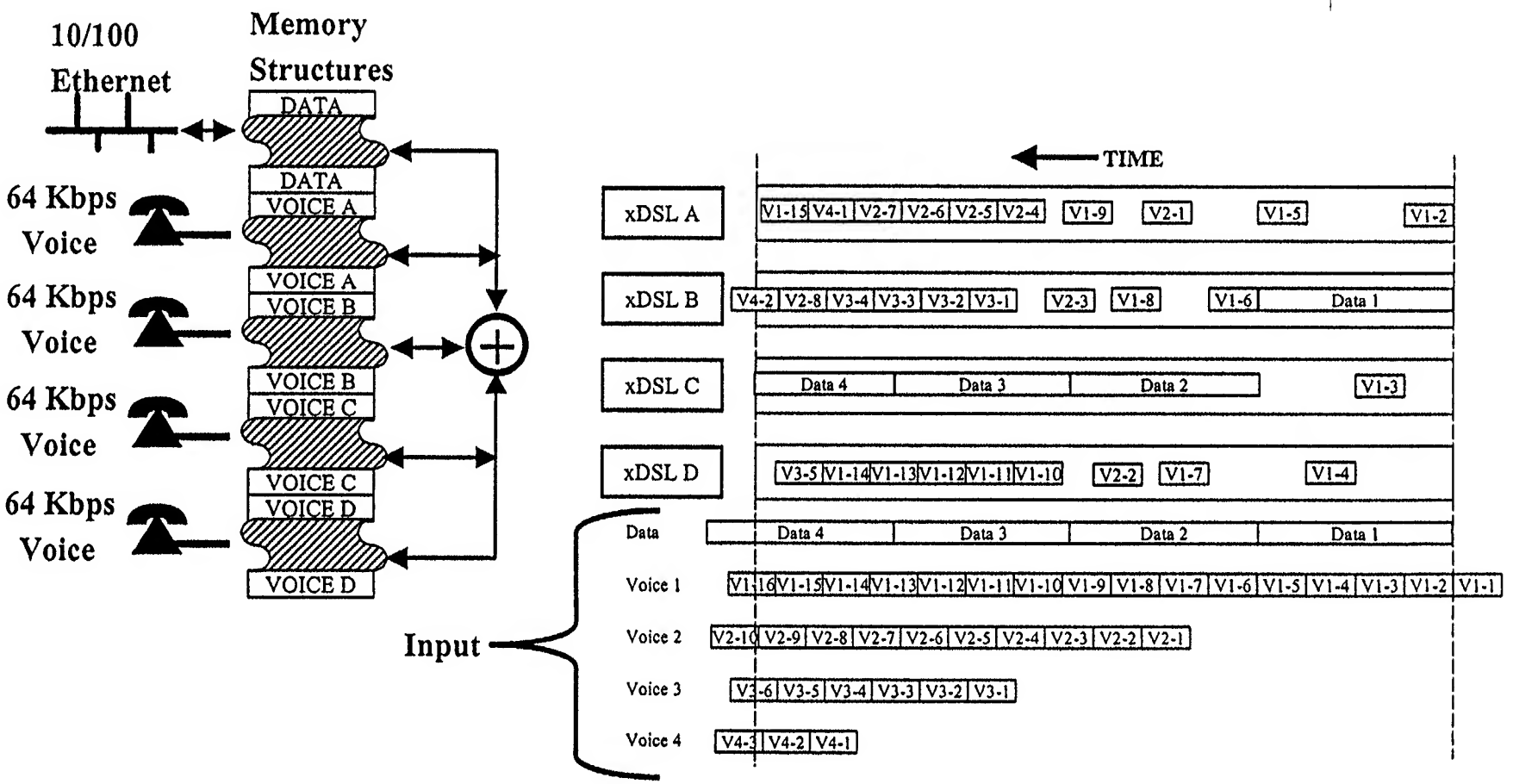


Figure 6

Figure 7


10/100
Ethernet
Memory
Structures
DATA
DATA
VOICE A
VOICE A
VOICE B
VOICE B
VOICE C
VOICE C
VOICE D
VOICE D
64 Kbps
Voice
64 Kbps
Voice
64 Kbps
Voice
64 Kbps
Voice
Input
TIME
xDSL A
V1-15 V4-1 V2-7 V2-6 V2-5 V2-4 V1-9 V2-1 V1-5 V1-2
xDSL B
V4-2 V2-8 V3-4 V3-3 V3-2 V3-1 V2-3 V1-8 V1-6 Data 1
xDSL C
Data 4 Data 3 Data 2 V1-3
xDSL D
V3-5 V1-14 V1-13 V1-12 V1-11 V1-10 V2-2 V1-7 V1-4
Data
Data 4 Data 3 Data 2 Data 1
Voice 1
V1-16 V1-15 V1-14 V1-13 V1-12 V1-11 V1-10 V1-9 V1-8 V1-7 V1-6 V1-5 V1-4 V1-3 V1-2 V1-1
Voice 2
V2-10 V2-9 V2-8 V2-7 V2-6 V2-5 V2-4 V2-3 V2-2 V2-1
Voice 3
V3-6 V3-5 V3-4 V3-3 V3-2 V3-1
Voice 4
V4-3 V4-2 V4-1

20020109h2h500F

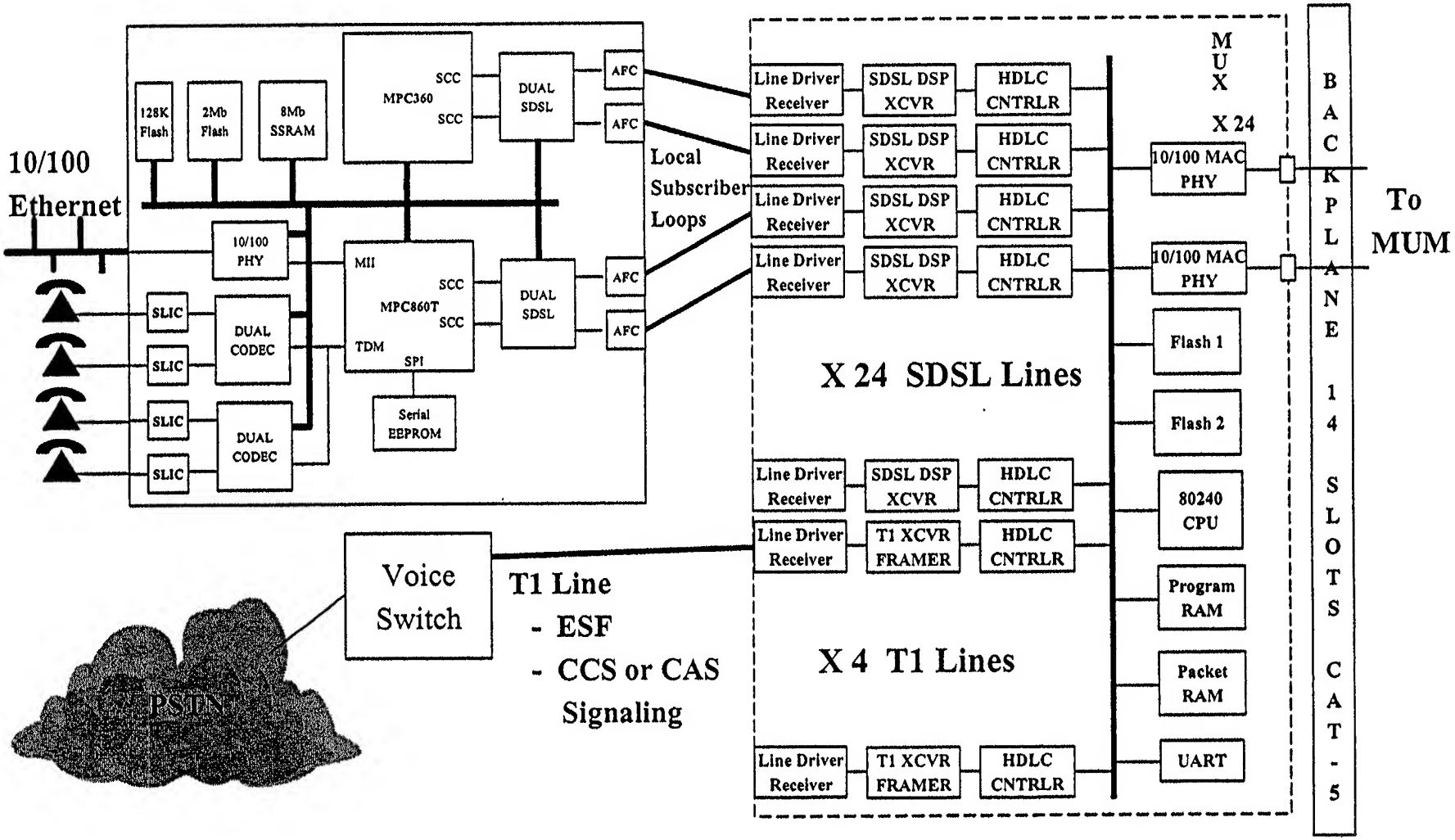


Figure 8